IN THE CLAIMS

Please amend the claims as shown below. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) A circuit for controlling the rise time of a signal, comprising:

a voltage multiplier which converts an input voltage to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal ; and

a divide by N counter coupled to said ramp generator.

2. (Original) The circuit of Claim 1, wherein said voltage multiplication circuit comprises a charge pump.

3. (Original) The circuit of Claim 1, wherein said signal is used to program and erase Flash EPROM cells.

4. (Cancelled)

5. (Original) The circuit of Claim 1, wherein said signal comprises a staircase ramp signal.

6. (Canceled)

7. (Previously Amended) The circuit of Claim 1 further comprising a level shifter.

8. (Original) The circuit of Claim 1 further comprising two non-overlapping clock signals.

9. (Previously Amended) The circuit of Claim 1 further comprising a ring oscillator coupled to said ramp generator.

10. (Previously Amended) The circuit of Claim 1 further comprising a capacitor divider network coupled to a switched capacitor network.

11. (Currently Amended) The circuit of Claim 10, wherein said switched capacitor network switches between ground potential and potential of a node of said capacitor divider network.

12. (Previously Amended) The circuit of Claim 11, wherein said node is coupled to a CMOS comparator.

13. (Cancelled)

14. (Currently Amended) A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor ;

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground potential and the potential of a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.

15. (Original) The switched capacitor controller of Claim 14, wherein said rise time is controlled according to a ratio of two capacitors.

16. (Original) The switched capacitor controller of Claim 14, wherein said on-chip generated voltage source is used to program a Flash memory.

17. (Original) The switched capacitor controller of Claim 14 further comprising an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump.

18. (Original) The switched capacitor controller of Claim 17 further comprising:

a divider coupled to said oscillator;

a non-overlapping two phase clock generator coupled to said divider.

19. (Original) The switched capacitor controller of Claim 14, wherein said ramp generator further comprises a capacitor divider network.

20. (Currently Amended) In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than voltage VCC from said power supply;

activating a program signal to program a cell of said flash memory;

generating a stair-case ramp based on said programming voltage in response to said program signal, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

21. (Currently Amended) The method of Claim 20 further comprising ~~the step of~~ switching a capacitor between ground potential and the potential of a node voltage to generate said stair-case ramp.